REMARKS

Claims 1, 3-14 and 16-24 are currently active.

Antecedent support for the amendment to the claims regarding the plurality of fabrics is found in figure 3.

The Examiner has objected to Claim 1. Claim 1 has been amended to obviate this rejection.

The Examiner has rejected Claims 9-13 and 18-24 under 35 U.S.C. 112, second paragraph. Claims 9 and 18 have been amended to obviate this rejection.

The Examiner has rejected Claims 1, 3, 4, 14, 16 and 17 as being anticipated by Sindu. Applicants respectfully traverse this rejection.

Referring to Sindu, there is disclosed a high-speed switching device. Sindu teaches in a packet switching system, a source 10 is connected to one or more routers 20 for transmitting packets to one or more destinations 30. Each router 20 includes an input switch 100, and output switch 102, a memory 104 including one or more memory banks 105, a

controller 106 and a plurality of input and output ports 107 and 108, respectively. Associated with the controller 106 is controller memory 109 for storing a routing table. Packets are received at input port 107, transferred to input switch 100 and stored temporarily in memory 104. When the packet is received by switch 100, a key is read from the first data block in the packet and transferred to controller 106. The key contains destination information which is derived from the header fields associated with the first block of data in a packet. A route lookup engine 110 and controller 106 performs a search based on the key information and returns a result which includes the output port associated with the destination. Output switch 102 transfers the notification to the identified output port 108. Upon receiving notification information, the output port 108 initiates the transfer of the packet from memory 104 through output switch 102 back to the appropriate input port 108. Each input port 107 includes a line input interface 300, a data handler 304 and a cell output port 306. Packets are received at line input interface 300. As the packets are received, data handler 302 divides the packets received into fixed length cells. As the data handler divides the incoming packet into fixed link cells, it synchronously outputs the cells to input switch 100 through cell output port 306. See column 4, lines 14-61.

Sindu teaches a single cell is transferred from input port 107 to input switch 100 at each cell slot. The data format for each cell transferred from an input port to input switch 100 includes an internal header and a cell data field. The input switch 100 includes a round

robin data handler 500, one or more input port interfaces, one or more memory interfaces, a like plurality of pointers, and output processor 505, one or more port interfaces, and a reservation table 508, an indirect cell processor, controller interface and read controller 516. Round robin data handler 500 receives cells for each input port and transfers them to output processor 505 for output to an appropriate memory bank 105 in memory 104. See column 5, lines 19-41.

Round robin data handler 500 and output processor 505 transfers cells out to memory 104 on transmission lines 460. Round robin data handler 500 time division multiplexes the transfers to output processor 505 such that consecutive cells from the same input port are written to consecutive memory banks 105 in memory 104. Round robin data handler 500 includes a key reading engine 514 for determining the key information associated with a first cell in a packet and a linking engine 515 for linking cells in the same packet. Linking engine 515 determines the starting address in memory for the first cell to a given packet. See column 6, lines 1-34.

As is apparent from the above description, there is no teaching or suggestion of the limitation of sending portions of the packet as stripes to each fabric, let alone there being a plurality of fabrics, as found at applicants' claimed invention.

Referring to Calamvokis, there is disclosed a cell switch fabric chip. Calamvokis teaches that the switch can be thought of as consisting of three main types of blocks. At the center there is the end-port switch core 20, each switch core port 21 operating at the same predetermined speed. Attached to each of the ports 21 is an adapter card 22. Each adapter card 22 interfaces a number of lower speed external switch ports 23 to a switch core port. Finally, there is a processor board 24 which performs signaling and virtual channel setup functions. See column 6, lines 1-10. Calamvokis teaches the switch core comprises a switch fabric 30 with input and output ports 37, 38 which are generally paired and as such constitute the switch core ports, a shared cell-body memory 31, the free address listed memory 32, a controller 33, and a communications block 34 for carrying out ATM adaption layer and other higher communication layers processing of cells intended for/coming from the controller (thereby enabling the ladder to communicate through the network of which the switch forms a part). The operation of the switch core is very simple. The input ports 37 are serviced in strict order one cell at a time. When a cell comes in on one of the input ports the fabric 30 writes the cell body into the shared cell body memory 31 at an address taken from the free address list memory 32. This address is also passed to the controller 33, along with the header of the cell to which it relates. Because the input ports 37 are serviced in a fixed order, the controller 33 can tell the source of the cell from the arrival time of the header. See column 6, lines 44-53.

As is apparent from the above description of Calamvokis, there is no teaching or suggestion of the limitation of sending portions of the packet as stripes to each fabric, let alone there being a plurality of fabrics, as found at applicants' claimed invention.

In regard to Petersen, Petersen teaches a sublayer 301 called the segmentation and reassembly sublayer. The segmentation and reassembly sublayer is invoked if a user data packet is so long that segmentation is necessary to avoid sending user data to a receiving entity and a minicell whose length, excluding the header, exceeds a predefined maximum length. See column 3, lines 23-32.

Petersen teaches a sending entity 401, an interconnecting link 402, and a receiving entity did 403. The sending entity contains the segmentation part of the segmentation and reassembly sublayer and a receiving entity contains the reassembly part of the segmentation and reassembly sublayer. The interconnection link carries the ATM cells from the sending entity to the receiving entity, and the ATM cells, in turn, carry the segment of the user data in minicells. See column 3, lines 33-44. Unlike the known ATM protocol model, there is no longer a 1-to-1 correspondence between each user data packet in each mini cell. Moreover, a single minicell can overlap no more than one ATM cell border as compared to the known protocol model. This is because the length of each mini cell, is limited to a length that is less than the ATM cell payload. See column 3, lines 45-56.

As is apparent from the above description of Peterson, there is no teaching or suggestion of the limitation of sending portions of the packet as stripes to each fabric, let alone there being a plurality of fabrics, as found at applicants' claimed invention.

Accordingly, the active claims are neither anticipated nor made obvious from Sindu, nor make obvious from Sindu in view of Calamvokis and Peterson.

In view of the foregoing amendments and remarks, it is respectfully requested that the outstanding rejections and objections to this application be reconsidered and withdrawn, and Claims 1, 3-14 and 16-24, now in this application be allowed.

CERTIFICATE OF MAILING

I hereby certify that the correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Assistant Commissioner for Patents, Washington, D.C. 20231

on 3/7/05

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